



-Using Clarinet for Analog Measurement -

1. INTRODUCTION

The data in any B-channel (basic or primary rate) can be directed to the analog/digital ports on the ISDN pod, or to the digital port (TRANSDATA interface).

These interfaces can be used as:

- permanent connections (Data Link, TRANSDATA, TRANSIT or the two Cofidec interfaces). The permanent connections are initialised upon profile launching and set for the entire duration of the profile.
- switched connections established by the Q931 simulator for outgoing and incoming communications.

2. ANALOG PORT

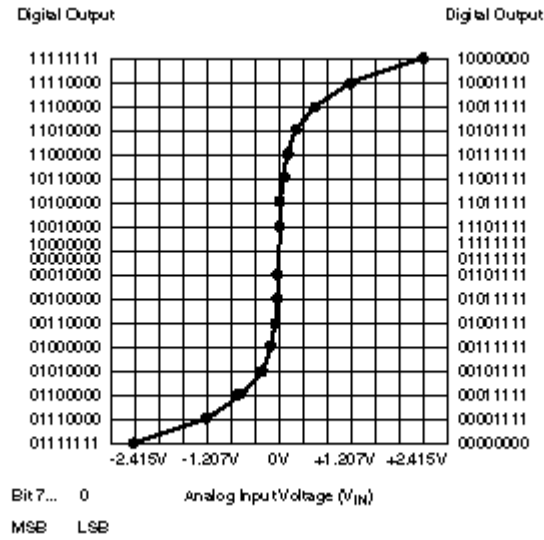
Main Characteristics:

- input impedance $\geq 100\text{k}\Omega$
- output level 0dB, on a 600Ω resistive load

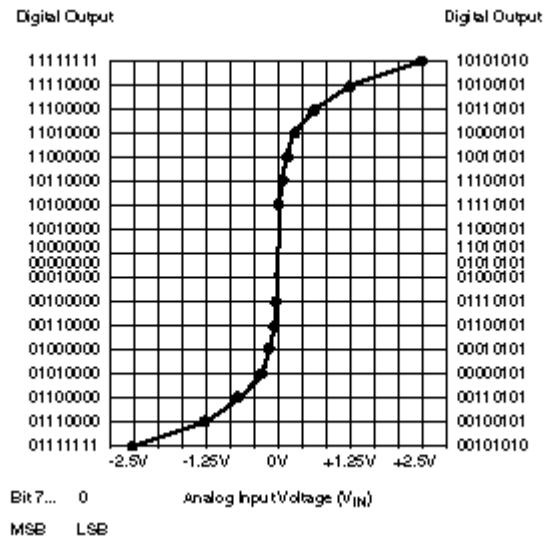
The analog port uses standard integrated filter Cofidec from Mitel (MT8965 for A-Law). But the analog I/O lines are routed through an analog switch array and output buffers which can introduce little additional distortion. Unfortunately, ACACIA doesn't provide any global performance data-sheet about analog I/O port because only functional tests are done during manufacturing.

The characteristics of the Cofidec are given hereafter:

- μ law Transfer Characteristic:



- A law Transfer Characteristic:



AC Electrical Characteristics - Transmit (A/D) Path - Voltages are with respect to GNDD unless otherwise stated. $T_A=0$ to 70°C , $V_{DD}=5\text{V}\pm 5\%$, $V_{EE}=-5\text{V}\pm 5\%$, $V_{REF}=2.5\text{V}\pm 0.5\%$, $\text{GNDA}=\text{GNDD}=0\text{V}$, Clock Frequency = 2.048MHz , Filter Gain Setting = 0dB . Outputs unloaded unless otherwise specified.

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Analog Input at V_X equivalent to the overload decision level at the codec	V_{IN}		4.829 5.000		V_{FP} V_{FP}	Level at codec: μ -Law: 3.17 dBm0 A-Law: 3.14 dBm0 See Note 6
2	Absolute Gain (0dB setting)	G_{AX}	-0.25		+0.25	dB	0 dBm0 @ 1004 Hz
3	Absolute Gain (+1dB to +7dB settings)		-0.35		+0.35	dB	from nominal, @ 1004 Hz
4	Gain Variation With Temp	G_{AXT}		0.01		dB	$T_A=0^\circ\text{C}$ to 70°C
	With Supplies	G_{AXS}		0.04		dB/V	
5	Gain Tracking (See Figure 12) CCITT G712 (Method 1)	GT_{X1}	-0.25		+0.25	dB	Sinusoidal Level: +3 to -20 dBm0 Noise Signal Level: -10 to -55 dBm0 -55 to -60 dBm0
			-0.25 -0.50		+0.25 +0.50	dB	
	CCITT G712 (Method 2) AT&T	GT_{X2}	-0.25 -0.50 -1.50		+0.25 +0.50 +1.50	dB dB dB	Sinusoidal Level: +3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
6	Quantization Distortion (See Figure 13) CCITT G712 (Method 1)	D_{QX1}	28.00			dB	Noise Signal Level: -3 dBm0 -6 to -27 dBm0 -34 dBm0 -40 dBm0 -55 dBm0
			35.60			dB	
			33.90			dB	
			29.30			dB	
			14.20			dB	
	Quantization Distortion (cont'd) AT&T (See Figure 13)	D_{QX2}	35.30 29.30 24.30			dB dB dB	Sinusoidal Input Level: 0 to -30 dBm0 -40 dBm0 -45 dBm0
7	Idle Channel Noise	C-message	N_{CX}		18	dBm0	μ -Law Only
		Psophometric	N_{PX}		-67	dBm0p	CCITT G712
8	Single Frequency Noise	N_{SFX}			-56	dBm0	CCITT G712
9	Harmonic Distortion (2nd or 3rd Harmonic)				-46	dB	Input Signal: 0 dBm0 @ 1.02 kHz
10	Envelope Delay	D_{AX}			270	μs	@ 1004 Hz
11	Envelope Delay Variation With Frequency	D_{DX}		60 150 250		μs μs μs	Input Signal: 400-3200 Hz Sinewave at 0 dBm0
12	Intermodulation Distortion	CCITT G712 50/60 Hz	IMD_{X1}		-55	dB	50/60 Hz @ -23 dBm0 and any signal within 300-3400 Hz at -9 dBm0
		CCITT G712 2 tone	IMD_{X2}		-41	dB	740 Hz and 1255 Hz @ -4 to -21 dBm0. Equal Input Levels
		AT&T	IMD_{X3}		-47	dB	2nd order products
		4 tone	IMD_{X4}		-49	dB	3rd order products
13	Gain Relative to Gain @ 1004 Hz (See Figure 10)	≤ 50 Hz	G_{FX}		-25	dB	0 dBm0 Input Signal Transmit Filter Response
		60 Hz			-30	dB	
		200 Hz		-1.8	0.00	dB	
		300-3000 Hz		-0.125	0.125	dB	
		3200 Hz		-0.275	0.125	dB	
		3300 Hz		-0.350	0.030	dB	
		3400 Hz		-0.80	-0.100	dB	
4000 Hz		-14	dB				
≥ 4600 Hz		-32	dB				
14	Crosstalk D/A to A/D	CT_{RT}			-70	dB	0 dBm0 @ 1.02 kHz in D/A
15	Power Supply Rejection	V_{DD}	$PSSR_1$	33		dB	Input 50 mV _{RMS} at 1.02 kHz
		V_{EE}	$PSSR_2$	35		dB	
16	Overload Distortion (See Fig. 15)						Input frequency=1.02kHz

* Typical figures are at 25°C with nominal $\pm 5\text{V}$ supplies. For design aid only; not guaranteed and not subject to production testing.

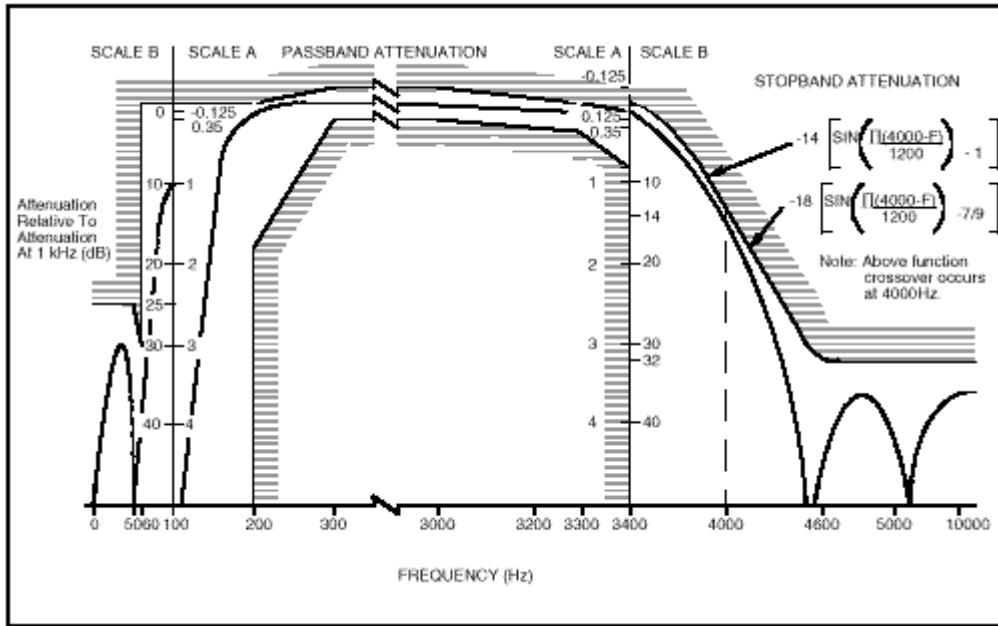
Note 6:
0dBm0=1.195 V_{RMS} for the μ -Law codec.
0dBm0=1.231 V_{RMS} for the A-Law codec.

AC Electrical Characteristics - Receive (D/A) Path - Voltages are with respect to GNDD unless otherwise stated.
 $T_A=0$ to 70°C , $V_{DD}=5\text{V}\pm 5\%$, $V_{EE}=-5\text{V}\pm 5\%$, $V_{RN}=2.5\text{V}\pm 0.5\%$, $\text{GNDA}=\text{GNDD}=0\text{V}$, Clock Frequency = 2.048MHz ,
 Filter Gain Setting = 0dB . Outputs unloaded unless otherwise specified.

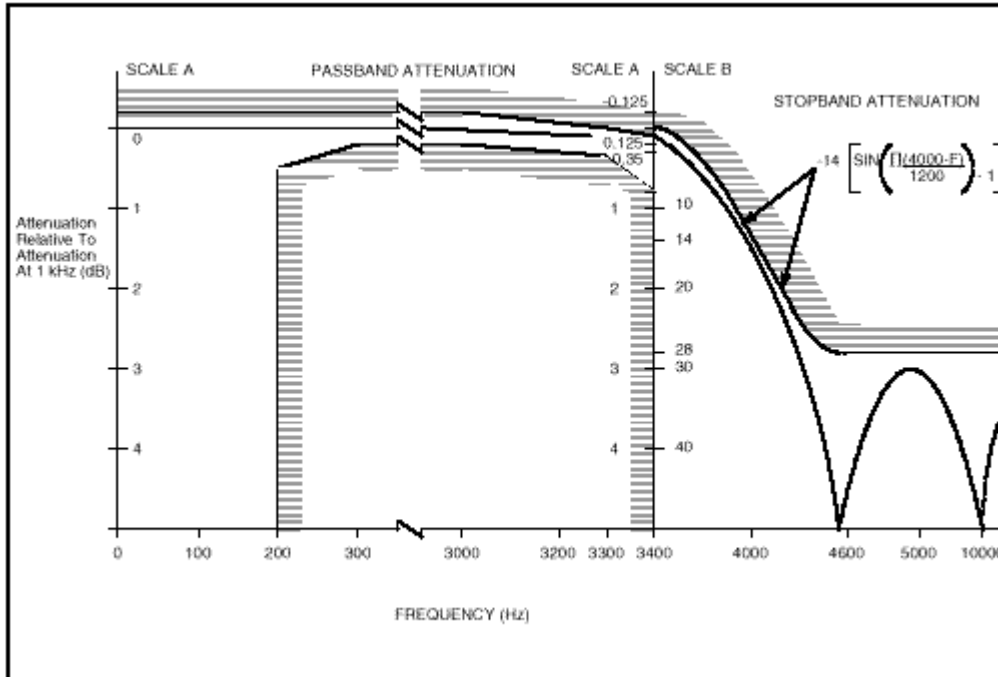
	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions	
A N A L O G	Analog output at V_R equivalent to the overload decision level at codec	V_{OUT}		4.829 5.000		V_{PP} V_{PP}	Level at codec: μ -Law: 3.17 dBm0 A-Law: 3.14 dBm0 $R_L=10\text{K}\Omega$ See Note 7	
	Absolute Gain (0dB setting)	G_{AR}	-0.25		+0.25	dB	0 dBm0 @ 1004Hz	
	Absolute Attenuation (-1dB to -7dB settings)		-0.35		+0.35	dB	From nominal, @ 1004Hz	
	Gain Variation	With Temp.	G_{ART}		0.01		dB	$T_A=0^\circ\text{C}$ to 70°C
		With Supplies	G_{ARS}		0.04		dB/V	
	Gain Tracking (See Figure 12)	CCITT G712 (Method 1)	GT_{R1}	-0.25 -0.25 -0.50		+0.25 +0.25 +0.50	dB dB dB	Sinusoidal Level: +3 to -10 dBm0 Noise Signal Level: -10 to -55 dBm0 -55 to -60 dBm0
		CCITT G712 (Method 2) AT & T	GT_{R2}	-0.25 -0.50 -1.50		+0.25 +0.50 +1.50	dB dB dB	Sinusoidal Level: +3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
	Quantization Distortion (See Fig. 13)	CCITT G712 (Method 1)	D_{QR1}	28.00 35.60 33.90 29.30 14.30			dB dB dB dB dB	Noise Signal Level: -3 dBm0 -6 to -27 dBm0 -34 dBm0 -40 dBm0 -55 dBm0
		CCITT G712 (Method 2) AT & T	D_{QR2}	36.40 30.40 25.40			dB dB dB	Sinusoidal Input Level: 0 to -30 dBm0 -40 dBm0 -45 dBm0
	Idle Channel Noise	C-message	N_{CR}			12	dBm0	μ -Law Only
Psophometric		N_{PR}			-75	dBm0p	CCITT G712	
8	Single Frequency Noise	N_{SFR}			-56	dBm0	CCITT G712	
9	Harmonic Distortion (2nd or 3rd Harmonic)				-46	dB	Input Signal 0 dBm0 at 1.02 kHz	
10	Intermodulation Distortion 2 tone AT & T 4 tone	IMD_{R2}			-41	dB		
		IMD_{R3}			-47	dB	2nd order products	
		IMD_{R4}			-49	dB	3rd order products	
11	Envelope Delay	D_{AR}			210	μs	@ 1004 Hz	
12	Envelope Delay Variation with Frequency 1000-2600 Hz 600-3000 Hz 400-3200 Hz	D_{DR}		90 170 265		μs μs μs	Input Signal: 400 - 3200 Hz digital sinewave at 0 dBm0	
A N A L O G	Gain Relative to Gain @ 1004 Hz (See Figure 11)	<200 Hz			0.125	dB	0 dBm0 Input Signal Receive Filter Response	
		200 Hz	-0.5		0.125	dB		
		300-3000 Hz	-0.125		0.125	dB		
		3300 Hz	-0.350		0.030	dB		
		3400 Hz	-0.80		-0.100	dB		
4000 Hz			-14.0	dB				
≥ 4600 Hz			-28.0	dB				
14	Crosstalk A/D to D/A	CT_{TR}			-70	dB	0 dBm0 @ 1.02 kHz in A/D	
15	Power Supply Rejection	V_{DD}	PSRR ₃	33		dB	Input 50 mV _{RMS} at 1.02 kHz	
		V_{EE}	PSRR ₄	35		dB		
16	Overload Distortion (See Fig. 15)						Input frequency=1.02 kHz	

* Typical figures are at 25°C with nominal $\pm 5\text{V}$ supplies. For design aid only; not guaranteed and not subject to production testing.
 Note 7: 0dBm0=1.185 V_{RMS} for μ -Law codec and 0dBm0=1.231 V_{RMS} for A-Law codec.

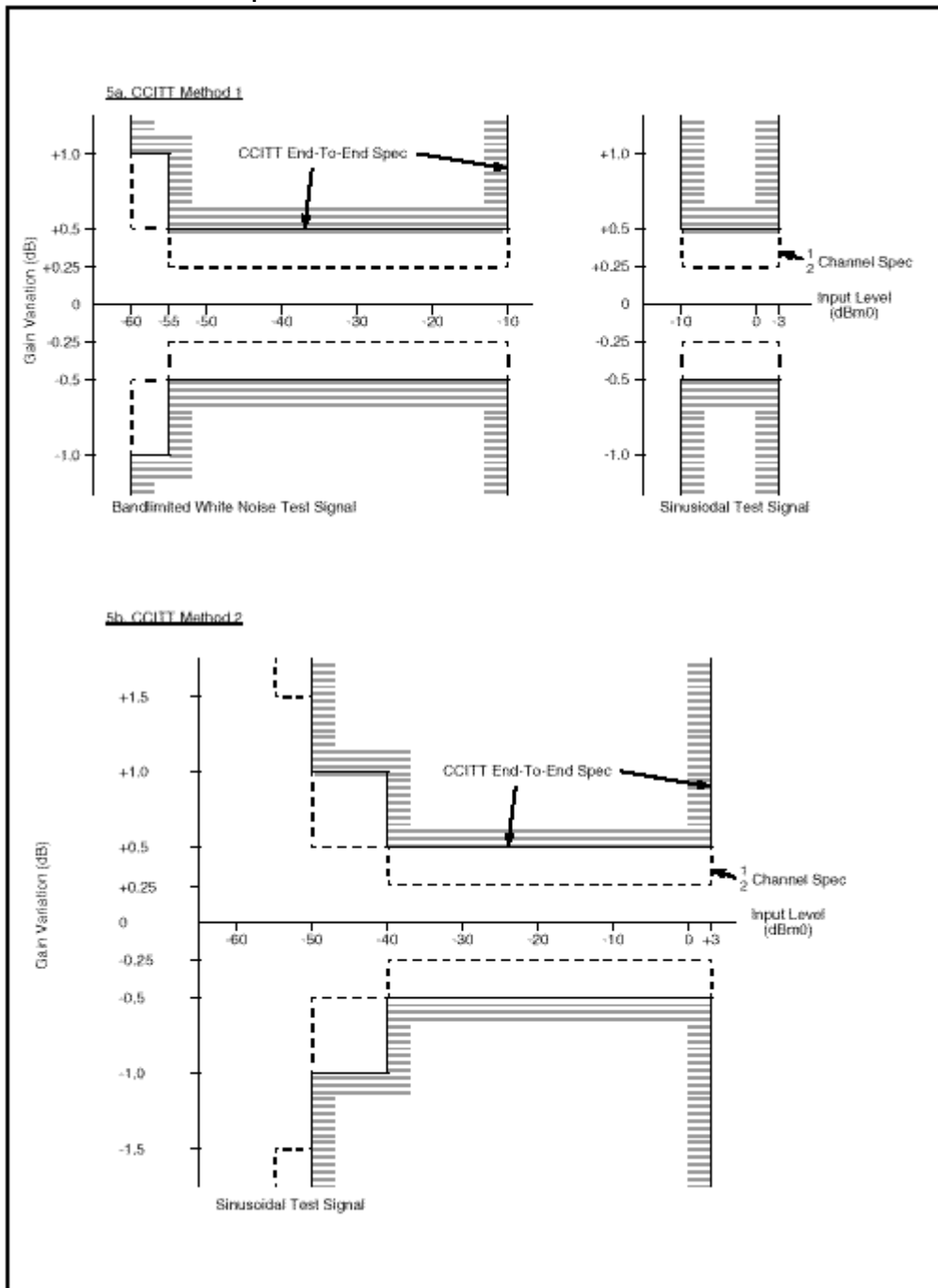
Attenuation vs Frequency for Transmit (A/D) Filter:



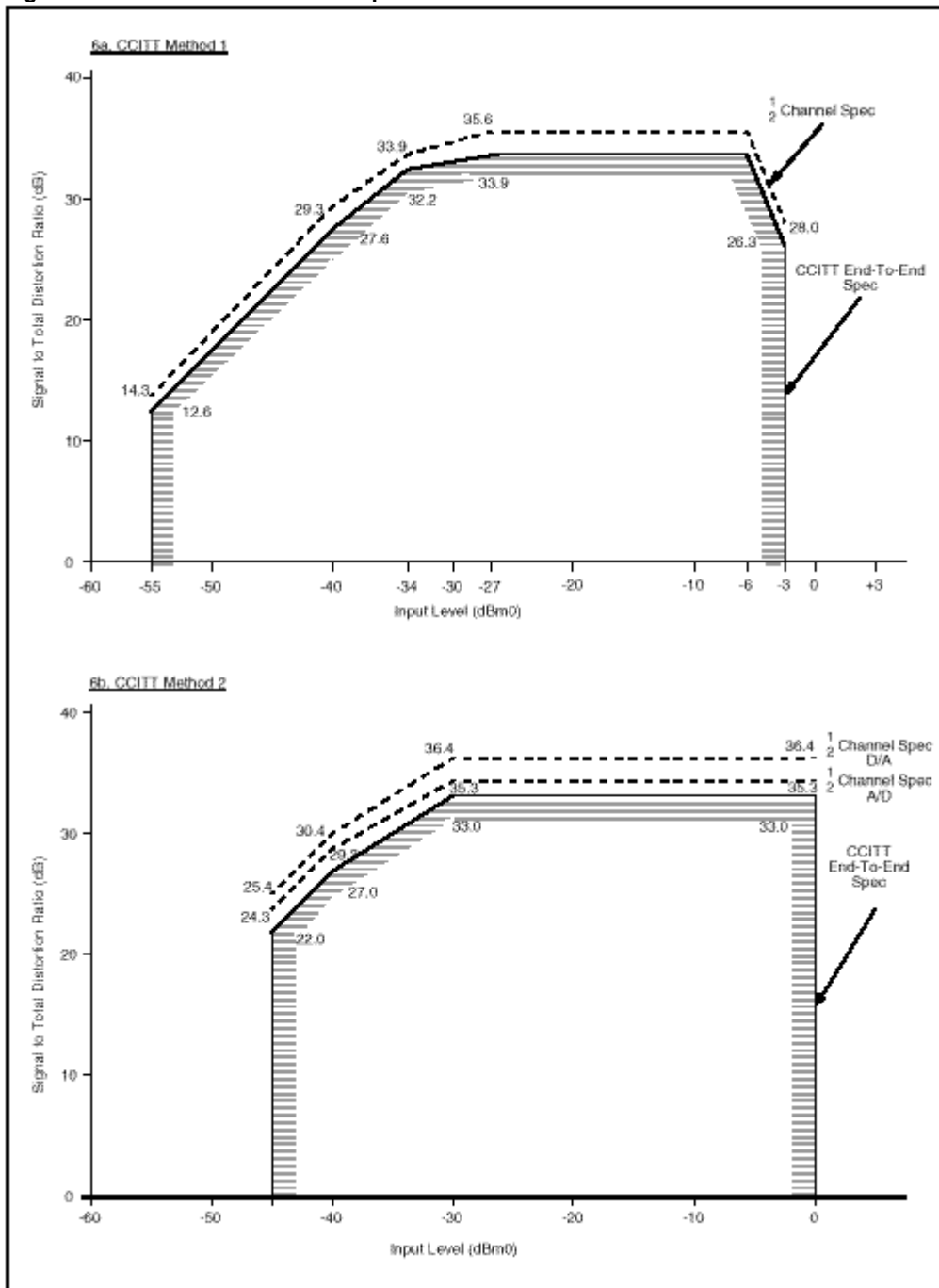
Attenuation vs Frequency for Receive (D/A) Filter



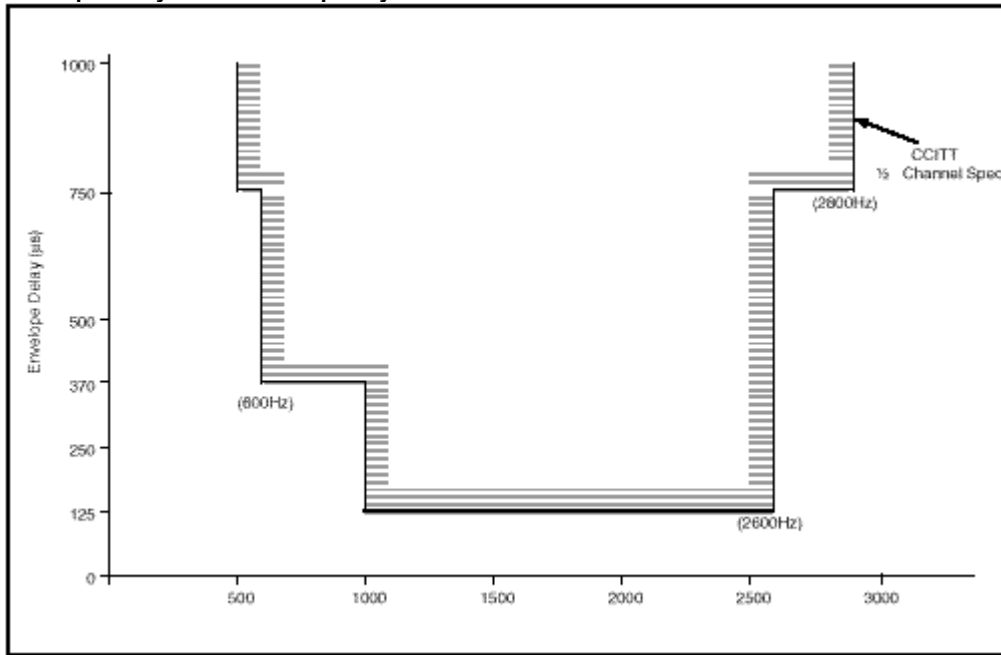
Variation of Gain With Input Level



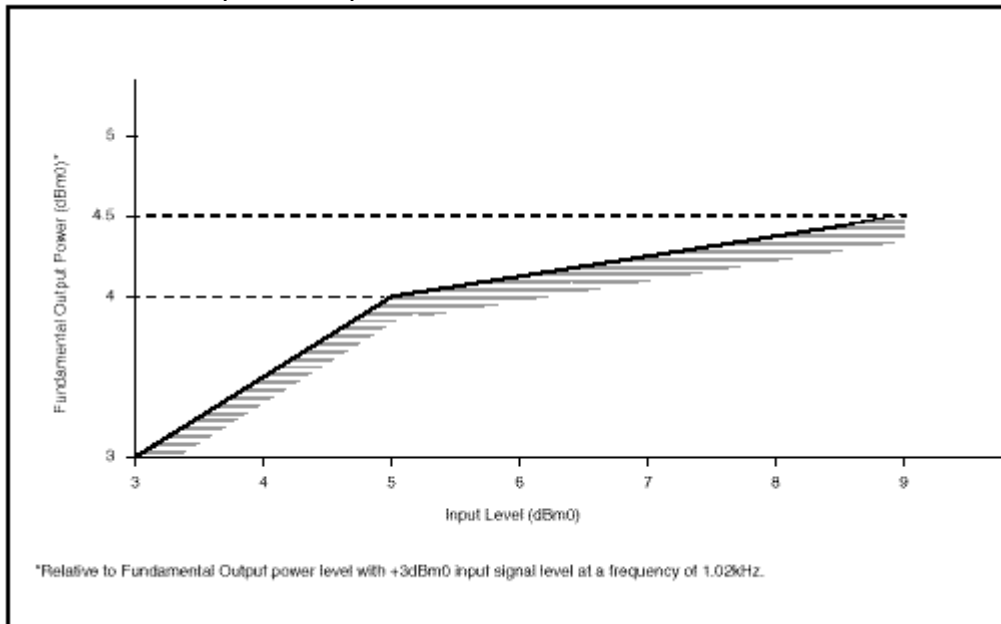
Signal to Total Distortion Ratio vs Input Level



Envelope Delay Variation Frequency



Overload Distortion (End-to-End)



3. TRANSDATA PORT

To make high-precision analog measurements, the digital interface (TRANSDATA) can be used to connect an high-precision external CODEC. Functional characteristics are based on ITU X24, electrical characteristics are defined by ITU V11 and mechanical characteristics are defined by ISO 4903.

The pod is a DCE, it provides timing information: S clock for signal element timing and B clock for byte timing. It operates in "burst isochronous" operation with a nominal bit rate of 2048kbits/s: R/T transitions occur on OFF/ON transition of the S clock, R/T are sampled on ON/OFF transition of S.

In normal "simulation mode" R is an output and T an input, in "analysis only mode" R and T are outputs. The S clock is held in the ON condition during idle time.

4. CONCLUSION

The solution chosen to make analog I/O measurement with CLARINET depends on the precision required. The highest accuracy will be achieved when using an external high-precision CODEC.